ABSTRACT

A T-RAM array having a plurality of T-RAM cells is presented where each T-RAM cell has dual devices. Each T-RAM cell is planar and has a buried vertical thyristor and a horizontally stacked pseudo-TFT transfer gate. The buried vertical thyristor is located beneath the horizontally stacked pseudo-TFT transfer gate. A method is also presented for fabricating the T-RAM array having the buried vertical thyristors, the horizontally stacked pseudo-TFT transfer gates and the planar cell structure.